Fabrication and Measurement of One-Dimensional Transmission Stip-Line Resonators

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Abstract

In this thesis work we outline and detail our research into Cavity Quantum Electrodynamics, specifically with the use of a Coplanar Waveguide design. We describe our techniques for fabrication of quantum cavities using superconducting metals, both aluminium and niobium. We also describe the experimental measurements made on the niobium quantum cavities. For cavities with coupling capacitors of length 50 $\mu$m we received a Q-factor of $40 \cdot 10^4$ and for cavities with coupling capacitors of length 100 $\mu$m we received a Q-factor of $5.5 \cdot 10^4$. We also examine the power dependency of our resonance peak and investigate some non-linear effects due power as well as magnetic and temperature effects. We follow by discussing some of the possibilities for the future, including placing a qubit inside our cavity.
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Part I

Motivation and Theory
Chapter 1
Cavity Quantum Electrodynamics

One of the great aims of modern physics research today is in developing the quantum computer. One can imagine that the quantum computer would revolutionise our world, much as the advent of the traditional computer did in the latter half of the last century. Such technology would allow us at the very least to perform calculations in a fraction of the time it takes now, create encryptions that may never be broken and push our civilisation into another golden age of computing. This technology will make use of revolutionary ideas in physics which have been investigated for the best part of a century and which embody the delicate beauty and elegance of our universe. Much research has already been done in trying to develop this technology and in our organisation, we hope also to make a contribution to this exciting field.

One of the ways in which physicists are trying to create quantum circuits for quantum computing is through the field of cavity quantum electrodynamics or cQED. This involves coupling a two level system, such as an atom, to the vacuum state of the electric field inside a resonance cavity. The two level system is our quantum circuit and the vacuum state is the zero energy quantum state of the electric field in the cavity and contains no particles. It is denoted by $|0\rangle$ or $|\rangle$. What has been experimentally predicted and shown is that in the presence of an atom (or other two level system) the empty cavity transmission resonances split in what is called vacuum-field Rabi splitting [1]. We can couple photons to transitions in our two-level system by using a superconducting resonator with a very high quality or Q-factor. The Q-factor is $Q = \frac{\omega}{\Delta \omega}$ where $\omega_0$ is the resonance frequency and $\Delta \omega$ is the full width at half maximum of the resonance peak.

In order for strong coupling to occur we desire that the vacuum Rabi splitting due to the two level system must exceed the mean values of the decay rates of the cavity and the two level system [1]. Therefore we want a high Q-factor with a very small mode volume, $V$. So the Q-factor indicates the amplitude of the resonance, with a higher Q indicating a greater amplitude than a lower Q.
Therefore, the Q-factor is a measure of how sharp the resonance peak is. The coupling of the quantum circuit to the cavity resonance is described by the Jaynes-Cummings Hamiltonian

\[ H = \hbar \omega_r (a \dagger a + \frac{1}{2}) + \frac{\hbar \Omega}{2} \sigma^z + \hbar g (a \dagger \sigma^- + \sigma^+ a) + H_\kappa + H_\gamma \]  

(1.1)

where \( \omega_r \) is the cavity resonance frequency, \( \Omega \) is the atomic transition frequency and \( g \) is the strength of the atom-photon coupling. In order for strong coupling to occur, the Rabi splitting, \( 2g \), due to the two level system must exceed the mean decay rates of the cavity, \( \kappa = \frac{2\gamma}{T} \) and of the two level system \( \gamma \). [1], [2], [3]

where \( \nu_0 \) is resonant, or centre, frequency and \( \Delta \nu \) is the bandwidth.

### 1.1 Two-Level System

One of the difficulties with creating a quantum circuit is the isolation of it from the outside environment. Interaction with the outside environment can cause destruction if the superposition state and thus loss of information. Therefore it is important for us to be able to preserve the state from depleting and relaxing, in order to carry and extract the information. This is why strong coupling is so desirable, as it causes the desired isolation of the quantum circuit.

The quantum circuit used by a group at Yale University [4] was the Cooper Pair Box (CPB). This consists of a superconducting 'island' which is coupled by one or more Josephson tunnel junctions to the ground plane of the cavity.[5]

This device is fabricated between the ground plane and centre conductor of the cavity and is a tunable system. It is described by the Hamiltonian

\[ H_a = -\frac{1}{2}(E_{cl} \sigma_z + E_J \sigma_z) \]  

(1.2)

where \( E_{cl} \) is the electrostatic energy and \( E_J \) is the Josephson energy of the circuit. Tuning of \( E_{cl} \) is done using the gate charge and \( E_J \) by applying a flux bias \( \Phi_b \). At this time our plan is to fabricate a similar CPB into our resonance cavity.

### 1.2 Design of the Cavity

The initial design of our cavity was based on the work done at Yale [4]. We used a coplanar waveguide (CPW) design with a narrow centre conductor flanked on either side by ground plane conductors. The central strip-line is where the quantum circuit will be placed. Input and output capacitors are found at either end of the cavity with identical parameters. The capacitors keep the impedance constant, in our case \( Z = 50\Omega \), and influence the Q-factor of the resonator. By loading the resonator with these capacitances we can obtain a loaded Q-factor \( Q_L \) from
\[
\frac{1}{Q_L} = \frac{1}{Q_{int}} + \frac{1}{Q_{ext}}
\]  

(1.3)

where \( Q_{ext} \), the external quality factor is given by

\[
Q_{ext} = \frac{\omega C}{G_{ext}}
\]

(1.4)

and \( G_{ext} = \frac{2R_L C_k^2}{1+R_L^2 Q_{ext}^2} \) with \( R_L \), the loading impedance being 50Ω, \( \omega = 2\pi f \) where \( f \) is the resonance frequency, \( C_k \) is the coupling capacitance and \( Q_{int} \approx Q_L \).

We tested capacitors with different parameters, the details of which are outlined in the measurements section. The capacitance per unit length, \( c \) is a function of the dielectric constant of the SiO₂ and the ratio of the width of the space between the ground planes to the thickness of the ground planes, \( r = \frac{w}{d} \).

These calculations and the design of the cavity were done as another Master’s Thesis and details are outlined in ref [9].

A dielectric constant of \( \varepsilon_r = 9.25 \) and \( c \approx 0.152 \ \text{pF}(\text{mm})^2 \) were calculated. The length of the cavity was chosen to be 22.9 mm which is a similar length to the cavity used in ref[yale] and is able to fit on the 5 x 5 resonator chip. From this, we were able to calculate the total resonator capacitance \( C = cl/2 = 1.74 \ \text{pF} \). [7]
Part II

Fabrication of Quantum Cavities
Chapter 2

Fabrication of Quantum Cavities

2.1 Overview of the Fabrication Process

We fabricated quantum cavities using two different metals, first with aluminium and then with niobium. Both metals were fabricated using electron beam lithography (or EBL). The Al chips were then further fabricated using a lift-off technique and the Nb, using a dry etching technique. The first part of this chapter will explain how the electron beam lithography was used since the technique is similar for both the Al and Nb. The rest of the chapter will detail the lift-off and etching techniques and finally the bonding process will be described.

We began with a silicon wafer, which had been passivated by a layer of silicon oxide to the depth of 1 μm. We used electron beam lithography in two ways to create our structures. For the Al, we used electron beam lithography to create an evaporation mask out of film of polymer on the wafer, known as resist. We then deposited the Al into the gaps of resist, removed the resist and were left with our structure. For the Nb, we first sputtered the wafer with a layer of Nb, then covered the Nb with resist. Electron beam lithography was then used to create the reverse of the pattern written for the Al and we etched the chip. Figs 2.1 and 2.2 show the designs for each type of cavity.

2.2 Electron Beam Lithography

Electron beam lithography (e-beam lithography or EBL) is a method by which we are able to create a mask for the deposition of materials onto a chip or a mask for etching. Positive electron beam resist is used in our research which is a polymer which suffers bond-breakage when bombarded with electrons. Negative electron beam resist would create bonds with other polymer chains when bombarded and is used to create the opposite pattern of that made with the
Figure 2.1: Al cavity design. The inset shows detail of the finger capacitors. The fingers are 50 $\mu$m in length.

positive resist).

The structures made in this project were done using the Raith 150 TurnKey system. This system uses a scanning electron microscope (SEM) created by LEO Electron Microscopy Ltd with a Gemini column and has a high precision laser interferometer stage. Our pattern was written using a computer aided design (CAD) program which is part of the Raith operating software. This design was done as part of a previous research project. [6]

2.2.1 Preparing the Resist

E-beam resist consists of long polymer chains which are dissolved in a solvent. It comes in liquid form which is poured onto a spinning wafer and then baked to make solid. The spinner spins the wafer at two speeds, a slower speed during which we pour on the resist and a much faster speed which spreads the resist into a thin layer on top of the wafer.

For the Al cavities we used two layers of resist; PMGISF7 (the lower layer) and a Zep 520A/Anisole (1:2) combination (the upper layer). To create a 400 nm thick layer of PMGISF7, we spun the resist onto our silicon wafer at a speed of 1200 rpm and then baked it for 10 mins at a temperature of 180°C. To create
Figure 2.2: Nb cavity design. The capacitance fingers are 50 μ in length here also

the upper layer, with a thickness of 60 nm we spun at a speed of 2400 rpm and baked for 10 mins at the same temperature as for the PMGI. Using two layers creates an undercut of resist which can be useful when evaporating.

For the Nb cavities we used 10 cm² silicon wafers which were argon sputtered with 200nm of niobium at the Chalmers Institute of Technology by Alexy Pavlotsky. The Nb coated wafers were spun with a 330nm layer of undiluted ZEP520A. We spun the resist at a speed of 6000 rotations per minute for 60 seconds and then baked it for 10 mins at 180°C.

It is important when spinning to make sure the wafer is clean and that it is centered on the spinner to create an even, smooth layer of resist. Also, when pouring on the resist, hold the neck of the bottle close to the wafer so that air bubbles don’t become trapped in the resist. The best resist is in the centre of the wafer since it can build up at the edges, creating an uneven surface which may be thicker than desired. For this reason, if one’s sample is very sensitive to the thickness of the resist, such as when creating structures on the nanometre scale, it is useful to be able to spin the whole wafer and use the centre part for the samples. For creating our quantum cavity however, this was not extremely important as we have a large feature size. Fig. 2.3 shows the chips, covered with resist being written with the e-beam.
2.2.2 Developing the Resist

After exposing to the e-beam, it is necessary to develop the resist. For the Al cavities, the ZEP520A/anisole layer is developed by immersing the chip into P-Xylene and the PMGISF7 layer is developed in a mixture of MF322 and water (in the proportions 9:6). Deciding on the best development times took a little experimentation. Although the quantum cavity can withstand a certain amount of overdevelopment, under-developing the ZEP/anisole layer meant that it did not dissolve completely and meant that when the bottom layer was developed, the upper layer created bubbles and flaps of material that destroyed the structures as can be seen in fig. 2.4.

Too much development of the bottom layer causes too much undercut which can cause the structure to collapse in on itself. After trial and error, we found the optimum time for development of the top layer was 1 minute and 30 seconds and for the bottom layer was 2 minutes 30 seconds for the electron dose that had been used for writing the pattern.

For the Nb chips we developed the exposed, undiluted-ZEP 520A resist using P-Xylene. Overdevelopment leads to a broadening of the structures so that after etching the cavity areas will be too wide and the capacitance fingers will be too narrow. After trial and error we found the optimum time was 2 minutes 30 seconds.

The chips on which we exposed were 5 x 5 mm in size. The quantum cavity itself is quite a large structure and so it was necessary to use the 120 μm aperture of the e-beam system, giving a current of approximately 4 nA. The width of the cavity spaces is 4 μm. The write-field is 1 mm², the magnification is x 70 and the dose is 49 μAs(cm)⁻². We used the same parameters for writing both
the Al chips and the Nb chips. The large structure meant that while good focusing and stigmation are always desirable, they are not vital in our case. However, the large structure and especially the large area it covers caused some problems, especially with regards to contamination. Methods of overcoming these problems are outlined below.

2.2.3 Using the 120 μm Aperature

The large pattern was far too large for one write-field and therefore stitching of the write-fields was needed. To guarantee that there would be no interruption of the conductors at the stitching boundary we created "stitching pads" using an extra layer of dose, slightly offset from the main pattern, to cover over the stitching boundary. This meant that write-field alignment was very important and somewhat challenging for such a large aperture, especially since it has been difficult to create good high-definition contamination marks for write-field alignment since the start of this project. The lack of contamination marks presented a challenge when doing write-field alignment. Instead we had to use contaminants on the chip, such as flakes of Si. However, we were trying to keep our chips extremely clean and so there were not many contaminants. At one point, we were using features at the edge of the chip for focusing and write-field alignment and then later on, scratching a piece of Si chip with the diamond pen and then touching the tip to the surface in the area where we intended to do our focusing and write-field alignment. In this way, we could deposit flakes of Si onto areas where they would not interfere with our structures. The quality of the write-field alignment varied with the use of these methods and also due to our using a 1 mm² write-field but was always successful in that there was a well defined gap with no shorting of the chip at the stitching boundaries.
2.2.4 Challenges with Creating a Large Structure

With the cavities, the biggest challenge with dealing with such a large structure was in trying to keep it clean. A small piece of Si flake or undissolved resist settled in the gaps between the waveguides could potentially short the whole structure, either by being covered with Al or by acting as an etch stop, which was allow unwanted Nb to remain. Since these gaps ran unbroken over such a large area, there was a high probability of this occurring, which necessitated some extremely careful handling of the wafer and chips, to minimise this risk. Every care was taken to protect the chips from dirt, including handling them only under the evacuation hood, cleaning with ionised and distilled water and immersing the chips in the sonic bath for a few seconds before loading into the e-beam. The chips were examined under the microscope before they went into the machine, to ensure that the chip was clean. After placing in the sample holder they were blown with the nitrogen gun one more time before loading. The nitrogen gun was used to blow debris off of the chips and is very clean. Chips were handled as little as possible and only ever with clean tweezers and wearing latex gloves. Overall, these precautions could ensure most chips were clean enough to be evaporated or etched.

2.2.5 Using a Matrix of Chips in the E-beam

In order to process as many chips as quickly as possible, we set up the e-beam to expose a matrix of 3 x 3 chips. This matrix consisted of an e-beam-resist-covered 1.5cm square chip which had been scribed on the back side prior to exposure. The e-beam was then set up to repeat the cavity pattern in the required interval so that one could potentially have nine chips at the end. One of the problems with exposing over such a large area is that the focusing can vary over distances due to imprecise leveling of the stage. There is software in the Raith 150 that allows one to focus on three corners of the chip and the software calculates that...
angle of tilt of the chip in the z-direction. It is then able to adjust the e-beam’s focusing in different areas to compensate. Unfortunately, this software seemed to have a bug and we had trouble using it. Therefore, we disregarded this ability. The stage is very level right now and since accurate focusing is not vital to our pattern, we were able to create successful chips without using the software.

It is important that the lower edge of the chip is parallel with the bar on the sample holder so that the pattern is written in the correct place. This can be a little tricky to accomplish physically without contaminating the chip. The clamp must be placed very gently onto the chip so that small flakes of stainless steel from the clamp do not fly off and contaminate the chip. Also, once the clamp is down, the chip must not be moved, not even to rotate into a more desirable position, for the same reason as just outlined. The Raith 150 has an angle adjust feature that allows one to compensate for a chip that is not perfectly aligned. The system reads the positions of the corners of the chip on one edge and calculates how much the edge is misaligned. It then takes this angle into account when writing the pattern, thus ensuring that the pattern is in the correct position on the chip. Make sure to do the angle adjustment before doing the write-field alignment, otherwise all the write-fields will be tilted relative to one another.

2.3 Fabricating Al Cavities - Evaporation

After the pattern had been exposed, we evaporated the Al onto it. This was done in our Eurovac Deposition System. Because we were only evaporating pure Al onto the chip, and not having to oxidise it or perform angle evaporation, our procedure was quite straightforward.

First, we used the Oxford Plasma lab 80+ Reactive Ion Etcher (RIE) to
"ash" the sample in an oxygen plasma. The details of how the RIE works is outlined in Appendix B. "Ashing" involves using a very gentle plasma on the sample, to remove contaminants and undeveloped resist on the surface of the sample. It insures that the sample surface is clean before evaporating the Al onto it. We used a forward power of 10W, a chamber pressure of 100 mTorr and an oxygen flow of 20 secm for 25 seconds. Once ashed, the sample is ready for evaporation. The sample has to be placed onto the sample holder which holds it in place inside the evaporation system. It is important to put on a new pair of latex gloves at this point, since the sample holder will be put into the vacuum. Because we are not preforming angle evaporation, the sample can be placed in any orientation with respect to the holder. The holder and sample is then transferred into the vacuum chamber using the transfer rod. Once the transfer has been done successfully and the transfer rod retracted, we can start up the electron gun. For further information on using the Eurovac system, one can consult ref [8] for a detailed step-by-step guide.

We evaporated our samples with 500 nm of Al using this system. Lift-off of the unwanted Al is done using the remover chemical Microposot Developer 1165 which has been heated in a water bath of 55 degrees. Initially, we had some difficulty doing the lift-off successfully. We tried squeezing remover gently over the sample using a plastic syringe and by putting the sample into the sonic agitator for 10-15 second bursts. We found our samples were quite hardy and could take up to a minute of sonic agitation. We found lift-off was especially difficult near the "neck" of the waveguides, were they started to taper as can be seen in fig 2.8. We adjusted our CAD pattern a little by widening it, and this became less of a problem.

Only after lift-off was completed, did we break the chip into nine smaller chips. This was in order to prevent Si flakes from getting on the chip before deposition. Contaminants on the chip can result in lift-off of Al, rendering the structure useless as in fig 2.8. Also the Al covered dirt can short the chip if
Figure 2.8: Here we put the sample into the sonic agitator for extended lengths of time to see how much it could take. This was taken after it had been in there for more than a minute. As can be seen, we still did not have successful lift-off at the neck of tapers. Therefore, we widened this area which helped considerably.

is does not lift-off as shown in fig 2.6. An advantage of evaporating Al onto the whole matrix of chips is that it minimises the possibility of Al getting onto the edges of the individual chips, which could cause shorting of the structure through the Si chip. If Al does get onto the edges, one could sometimes remove it by gentle sanding, but this creates a lot of dust and Si flakes, some of which are charged and can adhere to the structure and perhaps causing shorts. It is therefore better to avoid getting the Al on the edges in the first place. We also modified our structure so that the waveguides did not extend completely to the edges of the chips and this helped considerably.

2.4 Fabricating Nb Cavities - Etching

Our initial experiments with Al cavities failed to find a sharp cavity resonance. We may simply have missed the peak but this failure resulted in a decision to switch to Nb. ref [6]. This time, the e-beam resist was exposed to a pattern which was the reverse of the pattern used for the aluminium, exposing the waveguide gaps as shown in fig 2.2. This had the additional advantage of very large ground planes, much larger than the ground planes on the Al chips. Another aspect of our Nb design is that it tries to compensate for the problems with breaking correctly. It is important that wafer is scribed as accurately as possible, so that it breaks in the correct place. To increase the chance of it breaking correctly, we adjusted the pattern so that it had a large "buffer area"
Figure 2.9: SEM image of the walls of the Nb cavity. As can be seen in this picture there is no unwanted undercut of the structure

over the scribe line. Since it has been scribed on the back side, we can’t see where the scribe line is and the buffer area is designed to increase the chance of it breaking in the correct place. Despite our best efforts, accurate scribing and breaking is difficult and we did lose some chips due to them breaking in the wrong place.

2.4.1 Etching with Reactive Ion Etching

Once the pattern had been exposed and developed the cavity was ready for etching. The remaining e-beam resist was now acting as an "etch stop" for the etcher which means that Nb in the gaps between the waveguides could be etched away, exposing the SiO$_2$. It is important at this stage that there are no contaminants sitting on the exposed Nb that could act as an etch stop and thus cause a short by not etching the desired parts. After researching many different ways of etching Nb, including both wet and dry etches we decided on using the Oxford Plasma lab 80+ RIE to etch with BC$_3$. This method had been used successfully on Nb alloys ref.[9] and so we were hopeful it would work on pure Nb. Further details on how the RIE works can be found in the Appendix. Before attempting samples with successful lithography, some tests were done on some of the less successful samples to try to get an idea of how much time and power would be needed to etch. Also, it was important to find out what
the etching rate of the e-beam resist would be so that we would not etch right through it before etching the parts we wanted to etch. After several tests and measurements using the profilometer to measure film thickness, we found an approx. 1:1 ratio of the etch rates for resist niobium. That was the reason that we used a resist layer of more than 300nm. Our ideal parameters were etching with a forward power of 200 W at 50 mTorr of pressure for 12 mins. We found that using the RIE had the pleasing effect of etching without creating undercut which we were trying to avoid. A SEM image showing this is found in fig 2.7. We wanted to avoid undercut since that might cause a short later on when we put our qubit circuit inside the cavity. In that case, we will be evaporating Al on to the chip which might not make contact with the correct structure if it is blocked by the undercut sides of the cavity as shown schematically in fig 2.11. This is one of the advantages of using a dry etch instead of a wet etch ref. [10].

There are several steps that need to be followed when using the BCl3 RIE. For our samples, we always etch with a silicon wafer over the cathode, as it seems to etch more cleanly this way and makes the plasma more stable. To insert the wafer, it is necessary to undo the screws of the quartz ring and lift the ring up. The wafer may be placed onto the metal cathode, being careful not to allow it to slide off. When the wafer is centered, replace the quartz ring and screw it into place. Then, place the samples to be etched onto the silicon wafer. The RIE etches the silicon as well as the samples and so Si wafer will have to be replaced periodically. Other advantages include the ease of using the RIE and being able to avoid using highly corrosive etch chemicals. [10]

2.4.2 Removing the Resist after Etching

After etching, we removed the remaining e-beam resist using the Oxford Plasma lab 80+ RIE and pure oxygen. We ashed the chips with a forward power of 100 W at 50 mTorr pressure for 6 mins.

It is possible to break the wafer at any point after e-beam lithography. How-
ever, when we are putting a qubit circuit in the cavity, it might be better to keep the cavity chips in a 3 x 3 matrix for as long as possible. This is because when we will be using EBL to create the qubit circuit and will need to spin another layer of resist onto the chips. The larger the wafer, the more even the resist layer will be which is very important for angle evaporation. For this reason, it would be useful to work with even larger matrices, 4 x 4 or 5 x 5.

The chips were rinsed in IPA to clean them and then they were ready for bonding. Bonding was done in the same way for both the Al and the Nb cavities. The only difference was that the Nb cavities have large ground planes and thus we were able to create many more bonds on the Nb chips which is advantageous.

2.5 Comparison of Fabrication of Al vs Nb Cavities

As explained above, there are many challenges in the fabrication processes for these two metals. The greatest challenge for creating the Al cavities ended up being trying to keep them clean and then breaking in the correct place. We had a rather low success rate of about 30% for these chips. The largest challenge with Nb however was the scribing and breaking. Although cleanliness was vital for the etching process, the chips did not seem to get as dirty as the Al ones. Also, the Nb chips had a smaller area that was "empty" after resist development and so dirt was less of a problem. Additionally, dirt could also be etched along with the Nb and so there was a chance that a dirty chip would still be usable. In general, Nb cavities were far easier to fabricate than the Al and were fabricated successfully about 80% of the time. The e-beam pattern also took a lot less time to write. The Nb chips are also easier to bond due to the larger ground planes and as noted in previous, comparative experiments between Al and Nb chips, the Nb cavities show less "back ground" transmission than the Al cavities when both are mounted in the same measurement set up. It would be interesting to compare the measurement results after having fabricated the Al cavities in the same way as we have fabricated our Nb cavities.
2.6 Bonding Chips into Measurement Packages

The final step in fabrication is bonding of the sample to a printed circuit, or PC board. We connected and soldered MMCX connectors to the PC board. The connectors have three prongs, the middle-most being the connector and the other two connect to the ground. It is important to make sure that middle prong is not connected by the solder to the other connectors or the chip will be shorted. Also, it is better to try to solder with a minimum amount of solder, so that there is plenty of space for the bonding wires. Any rough edges should be filed off afterwards as they make unwanted signal reflections during measurement. It takes a little practice to become good at the soldering which is best done under a steroscope magnification. After soldering and filing the board is cleaned with ultrasonic agitation in a propenal bath.

Bonding is done using a Kulicke and Soffa Model 4523D semiautomatic bonder. The sample is placed in the recess of the PC board using either glue or hot wax. 25 µm thick Al wires are used to bond the sample to the PC board. Once this is done, we are ready to begin measuring our sample.
Part III

Measurement of the Nb Cavities
Chapter 3

50 µm and 100 µm Coupling Capacitors

The first cavity that we measured had coupling capacitors that were 50 µm long. We took a frequency sweep of the cavity between 1 and 10 GHz while the cavity was superconducting. We decided to take a very detailed sweep so as not to miss any peaks and therefore used a very low bandwidth and let it run overnight. All measurements were made with a power of -55 dBm except where stated otherwise.

![Figure 3.1: Full Transmission Sweep](image-url)
Our sweep showed three very distinctive features as pictured in fig 3.1. We named these features peaks 1, 2 and 3 respectively and they are referred to in this way in the rest of this document. A detailed sweep around each of these features is shown in fig 3. Peak 1 is found at 3.008 GHz at our base temperature of 25 mK. We find the frequency of the peak changes with different temperature and magnetic field, which we discuss in greater detail later in this chapter. Peak 2 is found at around 6.203 GHz and peak 3 at 9.30 GHz. In previous experiments with a capacitance of 25 µm ref. [6] the resonance peak was found at around 3.003 GHz.

The upper line in fig 3.1 shows the transmission spectrum without any cavity. Peak 1 and 3 are about equidistant from this line and we can see that if peak 2 were turned upside down, it would be about equidistant also. As can be seen from fig 3, peaks 1 and 3 have a Lorentzian shape. The features are anomalous in shape as they each seem to have dip in transmission right next the peak when viewed on the logarithmic scale. This is most apparent in the resonance peak and it could be that the background transmission hides the shape of the features for the other two peaks. Interestingly, were to turn it upside down, it would have a shape similar to peak 1’s. It could be that some kind of non-linear effect that is causing these anomalies, perhaps from coupling to other modes or from some sort of internal reflection. If we assume that peak 1 is our resonance peak and that peak 2 is our first overtone, then the frequency of peak 2 is off of our expected value by only 0.1% where the value of peak two is taken at the minimum. Also, we find that peak 3 occurs at 0.1% away from where we would expect the second overtone to occur. Therefore, we are confident that peaks 2 and 3 are in fact the first and second overtones, however, why peak 2 has the shape it does remains an unsolved question at this time. Actually, the midpoint between the lowest and highest points on peak two occurs exactly where we would expect the first overtone to occur.

As can be seen from fig 4.1, the first peak is the clearest since the background does not come up so high and therefore we have been able to get the most accurate Q-value with this peak. We found the resonance peak Q-value to be $40 \times 10^4$ when using a least-square-fit to the Lorentzian using Matlab and the
Figure 3.3: Comparison of the resonance peak at different powers. The more noisy image was taken at a lower power. We can see quite clearly that skewing is less apparent at the lower power, indicating that skewing could be due to a non-linear effect because of too-high power. Note both curves have been normalised on a linear scale and therefore there are no units for transmission, since this is just a ratio of the powers

Formula for the Lorenzian line shape as given by $I(\nu) = A \frac{\nu^2}{(\nu^2 - \nu_0^2)^2 + \frac{Q^2}{4}} + C$

where $\nu_0$ is the resonance frequency, $A$ is the amplitude, $Q$ is the Q-factor and $C$ is a transmission constant.

We were unable to get a Q-value for the second peak because of its shape but for the third peak we have a Q-value of $15 \cdot 10^4$.

For the 100 mum coupling capacitors, we again found three peaks, again within 1% of where we had expected them to be. We conducted most of our analysis on the resonance peak and we found that it had a Q-factor of $5.5 \cdot 40 \cdot 10^4$. It was expected that the Q-factor would decrease in size due to the larger capacitance. This peak also showed the characteristic dip next to it that we had observed in previous measurements.
3.1 Power Measurements

When measuring the resonance peak for the 50μm coupling capacitor chips we found that it had a rather unexpected shape. Using a logarithmic scale in the vicinity of the peak we could see a significant dip in the transmission spectrum followed by a pulling of the peak in the opposite direction as shown in fig. 3.

We theorise that high power is causing a non-linear inductance which is pulling the resonance peak and fig. 3.3 supports this idea. A theory which might explain this behaviour is the Duffing Oscillator. [11] This theory is outlined in the theory section of this thesis. Careful measurements of a 100μm coupling capacitor chip further supported this idea.

We took detailed power measurements in the range of -5 to -48 dBm using 1 step intervals. The result of this measurement is shown in fig. 3. It can be seen that as the power increases, the peak pulls to the right and then starts to pull to the left. Finally at about -16 dBm the peak has entered the unstable region as predicted by the Duffing oscillator and the oscillator’s differential equation has two solutions. Further work will be done on this to see if we can simulate the observed behaviour using this theory. We also observed that the dip did not change at all with power dependence. It is unknown at this time what is causing it.
Figure 3.5: Fig. showing the temperature dependence of the resonance peak. The jagged line shows how the Q-value changes with temperature and the red line shows how the frequency of the peak changes with temperature.

3.2 Temperature Dependence

Our temperature dependence measurements for the 50 μm coupling capacitors are outlined in fig 3.5. As one can see, the Q-factor changes slightly with temperature and has a maximum at the temperature of 0.44 K. This trend also matches the data from ref (Frank) and from later measurements on the 100 μm coupling capacitors. The Q-factor deteriorates as the temperature is increased and we observed that the pulling of the peak decreases also. However, it could be that the pulling is being hidden by the lower quality peaks as the temperature is increased.

It is also apparent that the resonance peak’s frequency changes with temperature as is shown in fig 3.5. This had been observed in all measurements taken by us and by the group at Yale [4] who explained it as being due to temperature related inductance effects. [7]
3.3 Applied Magnetic-Field Dependence

The final step in the measurements was to apply magnetic fields to the cavity and observe how the resonance peak moves with different magnetic fields. It is important that this is the last step in our measurements since applying magnetic fields seems to introduce a permanent flux into the cavity, thus irreversibly changing the cavity from its original state.

For the 100 μm capacitor chips we swept the magnetic field from 0 G to 21 G, then back to -21 G and back up to 21 G. This was done in 0.5 G step increments. The magnetic field dependence for both the Q-factor and the resonance frequency are shown in fig. 3.3.

As can be seen, the Q-factor becomes completely suppressed with applied magnetic field and does not recover, even at zero magnetic field. It could be that the magnetic field is breaking down the superconductivity of the niobium. The resonance frequency also moves in quite a symmetrical manner with magnetic field, suggesting that there may be trapped fluxes influencing its frequency.

3.4 Future Work

There are several more experiments planned. We would like to do measurements with no capacitors and also with straight capacitors, where the capacitors would be about 500nm apart. When we have all of these results, we can examine which capacitance can give us the best Q-value. We can also determine the dependence of the frequency on applied magnetic field which will be vital knowledge for when we put in our two-level system and try to use the magnetic field to tune it.

Once we know what kind of cavity we are going to use for our experiments, it would be possible to switch over to photolithography, which is much faster than electron beam lithography. Photolithography works by exposing light sensitive resist to a particular mask which has been fabricated out of quartz in the desired
pattern. It is impractical to use such a system until we are sure of which design of cavity we are going to use. One of the advantages of using electron beam lithography is that we can make small changes to the design very easily.

When fabricating our two level systems it certainly would be advantageous to have 3 x 3 or larger matrices of chips. Therefore, when we spin new e-beam resist onto the matrix, it will be quite even. This is going to important since we will be using Al evaporation to put in our two-level system and angle evaporation will be dependent on a consistent resist.
Appendix A

Reactive Ion Etching

Reactive Ion Etching (RIE) is a method of etching that is very commonly used. It combines chemical and physical etching processes. It is often used because it produces very anistropic etch profiles or even a positively slanted profile (picture) something that we found desirable for our research. The RIE that we used was the Oxford (something), a parallel plate RIE. It consists of a reaction chamber of a conductive material which can be vacuum pumped and a metal sample platter which serves as an electrode. The chamber is electrically grounded and the platter is electrically isolated from the chamber. A plasma is created inside the chamber by feeding the desired reactive gases (in our case BCl₃) in through the top and then using radio frequency (RF) power to strike the plasma. The RF power causes an oscillating electric field which strips the gas of its electrons, thus creating the ion plasma. The electrons which bounce against the chamber walls are grounded away and have no further role. The electrons which strike the isolated platter however, build up on the platter creating a strong negative voltage there (can be up to a few hundred volts). This negative voltage tends to attract the now positive plasma, causing the ions to diffuse towards the platter and whatever sample is on the platter.

When the ions reach the sample they can react with it in two ways, a physical way and a chemical way. The physical process, ion bombardment, is where the accelerated ions literally knock the surface atoms out of the material. This method of ion bombardment is also commonly used for cleaning samples (ashing). The chemical etching process creates a new gaseous substance, which occurs by adsorption of the reactive ions with the surface atoms of the sample. This chemical process can be enhanced by the physical bombardment of ions which creates active etching sites on the material as it helps remove the material. Then if the vapour pressure is high enough, this gaseous substance is carried off when the chamber is evacuated, taking the surface atoms with it, thus etching the surface. The other way in which the ions etch the surface is a purely physical process where the accelerated ions literally knock the surface atoms out of the material. This method of ion bombardment is also commonly used for cleaning samples (ashing).
Bibliography


[8] www.nanophys.kth.se/

