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A sub-μs thermal time constant electrically driven Pt nanoheater: thermo-dynamic design and frequency characterization

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Metal nanowires can emit coherent polarized thermal radiation, work as uncooled bolometers, and provide localized heating. In this paper, we engineer the temperature dynamics of electrically driven Pt nanoheaters on a silicon-on-insulator substrate. We present three designs and we electrically characterize and model their thermal impedance in the frequency range from 3 Hz to 3 MHz. Finally, we show a temperature modulation of 300 K while consuming less than 5 mW of power, up to a frequency of 1.3 MHz. This result can lead to significant advancements in thermography and absorption spectroscopy. *Published by AIP Publishing*. [http://dx.doi.org/10.1063/1.4948979]

Metal nanowire resistors can provide localized heating, radiation emission, and bolometric detection up to very high modulation frequencies, while maintaining low power consumption, thanks to their small size. They support surface plasmon polariton modes[1,2] that can be thermally excited and provide spatial and temporal coherence of the emitted thermal radiation.[3,4] Sub-μm-width thin-film platinum (Pt) nanowires have been shown to emit coherent polarized thermal radiation,[5] with coherence lengths over 20 μm and enhanced emission efficiency,[6] as well as to work as uncooled bolometers.[7] Pt nanoheaters offer chemical inertness up to high temperatures, a linear relation between resistance and temperature over a wide range, low power consumption, and ease of integration in systems on chip. Pt nanoheaters have been studied under DC excitation,[5,6] but recent results show that electromigration due to high current density is their dominant failure mechanism, and that AC operation greatly increases their lifetime.[8] For applications such as high-frame-rate scanning probe thermography and on-chip infrared (IR) absorption spectroscopy, rapidly temperature-modulated nanoheaters can act as low-power pulsed emitters and are thus of growing interest.

Here, we present three designs of Pt nanoheaters for high-frequency operation and characterize their thermal impedance between 3 Hz and 3 MHz using an AC electrical measurement method.[9,10] We experimentally demonstrate MHz-rate electrical temperature modulation of nanoheaters.

Assuming a linear time-invariant thermal system, we can write its complex thermal impedance in the frequency domain as[10]

$$Z_{\mathrm{th}}(\omega_{\mathrm{th}}) = \frac{\theta(\omega_{\mathrm{th}})}{Q(\omega_{\mathrm{th}})}, \tag{1}$$

where Q is the applied heating and θ is the temperature response at angular frequency ω_{th}. In our case, the dominant heat dissipation process is thermal conduction to the substrate,[11] so we disregard cooling due to radiation and convection. Therefore, Z_{th} only depends on material properties and device geometry.

We drive the resistive nanoheater using the electrical circuit shown in Fig. 1 and thus, by applying electrical frequency ω, we produce a Joule heating oscillation at $\omega_{\mathrm{th}} = 2\omega$, in phase with the drive current. We do not assume the heating power to be constant over all frequencies, as often done in literature,[10,12,13] because, at the high frequencies required to observe the nanoheater's thermal cut-off, the delivered power is affected by parasitic electrical reactances of the drive circuit. Further, in our case, the large temperature oscillation significantly changes the resistance of the nanoheater, according to

$$R = R_0 + R_0\alpha(T - T_0), \tag{2}$$

where R_0 is the resistance at a reference temperature T_0 and α is the temperature coefficient of resistance (TCR) of the heater material.[14] Thus the heating power is

$$Q_{2\omega}(\omega) = \frac{1}{2}\mathrm{Re}\left[V_{1\omega}(\omega)I^*_{1\omega}(\omega)\right]. \tag{3}$$

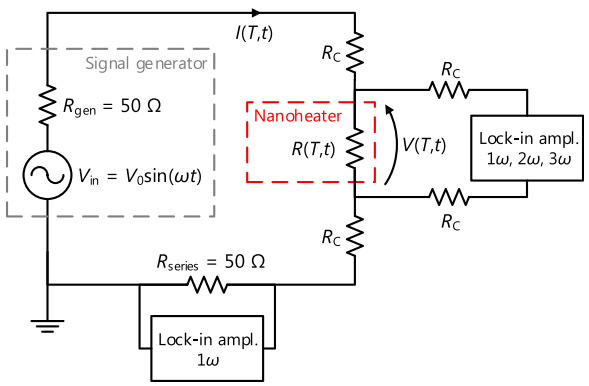

FIG. 1. The nanoheater is electrically connected in a four-wire configuration. Each connecting probe has a contact resistance R_C. The driving signal V_{in} is applied by a generator with 50 Ω output impedance. The first three harmonics of the voltage across the nanoheater and the first harmonic of the voltage across a 50 Ω series resistor R_{series} are measured with lock-in amplifiers.

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Here, V is the voltage across the heater and I is the drive current through it. As in any AC power system, the heating oscillates at 2ω around the average value of $1/2\mathrm{Re}[V_{1\omega}(\omega)I^*_{1\omega}(\omega)]$.

To evaluate θ, we exploit the fact that the oscillation of the nanoheater's resistance R with temperature at 2ω mixes with the driving current at 1ω, generating a third harmonic $V_{3\omega}$ in the voltage across the nanoheater. The complex temperature oscillation is

$$\theta_{2\omega}(\omega) = -2\frac{V_{3\omega}(\omega)}{\alpha R_0 I_{1\omega}(\omega)}. \quad (4)$$

This technique is referred to as the 3ω method[9,10] and has been used to characterize the thermal impedance of suspended Pt microwires[12] and carbon nanotubes[13] up to frequencies of 1 kHz and 50 kHz, respectively.

We aim to produce fast, power-efficient Pt nanoheaters by engineering their thermal impedance Z_{th} and hence their temperature dynamics. The silicon-on-insulator (SOI) substrate is a flexible platform well suited to this task because it provides two construction materials, silicon and silicon dioxide, with vastly different thermal conductivities, in a format that can be nanostructured by lithography. The thermal conductivity of bulk Si is[15,16] 148 W m K^{-1} and decreases by 0.33%/K from 300 K to 400 K. The thermal conductivity of bulk SiO_2 is about two orders of magnitude smaller,[17] 1.36 W m^{-1} K^{-1}, and increases by 0.10%/K from 300 K to 400 K. For thin films of Si[18] and SiO_2,[19] the conductivity values can be assumed to be slightly lower than the bulk values.

We present three nanoheater designs, depicted in Fig. 2. Design A has two thermally insulating SiO_2 layers and a single thermally conductive Si device layer without structuring. Design B has one SiO_2 layer and one Si layer, laterally insulated by a trench pattern cut through the Si and SiO_2 around the Pt. Design C has large parts of the Si layer and the SiO_2 layer under the heater removed, so that the remaining Si layer is suspended in air, to provide thermal insulation. The dimensions of the Pt nanoheater are identical for all designs: 3.5 μm long, 300 nm wide, and 60 nm thick.

The nanoheaters were fabricated by electron-beam lithography, Pt evaporation, and lift-off. A 7 nm thick chromium layer was deposited prior to the Pt to improve adhesion to the substrate. The substrate is an SOI wafer with a 220 nm thick Si device layer and a 2000 nm thick buried thermal oxide (BOX) layer. The upper 100 nm SiO_2 insulation layer in design A was deposited by plasma-enhanced chemical vapor deposition (PECVD). The layers were patterned using electron-beam lithography followed by plasma dry etching. In designs B and C, the BOX layer was etched by hydrofluoric acid (HF) vapor etching.

For characterization, the Pt nanoheaters were connected in a four-wire configuration: a sinusoidal driving voltage was applied across the two outer contacts, and the voltage drop was monitored at the inner two contacts.

First, we measured the TCR α of the Pt nanoheaters by heating the supporting substrate on a hotplate and measuring the DC resistance of the nanoheaters with a four-wire multimeter at different temperatures between 30 °C and 65 °C. The TCR measured 2.1×10^{-3} K^{-1} for all three designs.

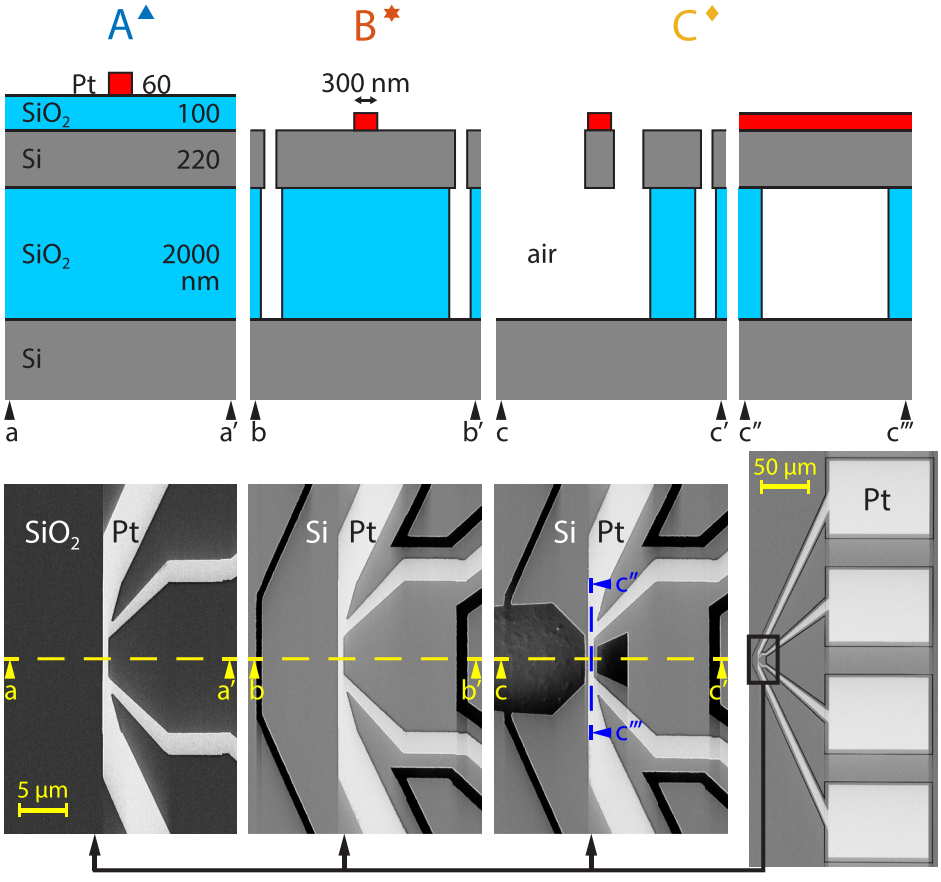

FIG. 2. Schematic cross-sections and top view scanning electron microscope (SEM) images of the three nanoheater designs. The rightmost SEM image shows the complete nanoheater pattern, including the contact leads and pads.

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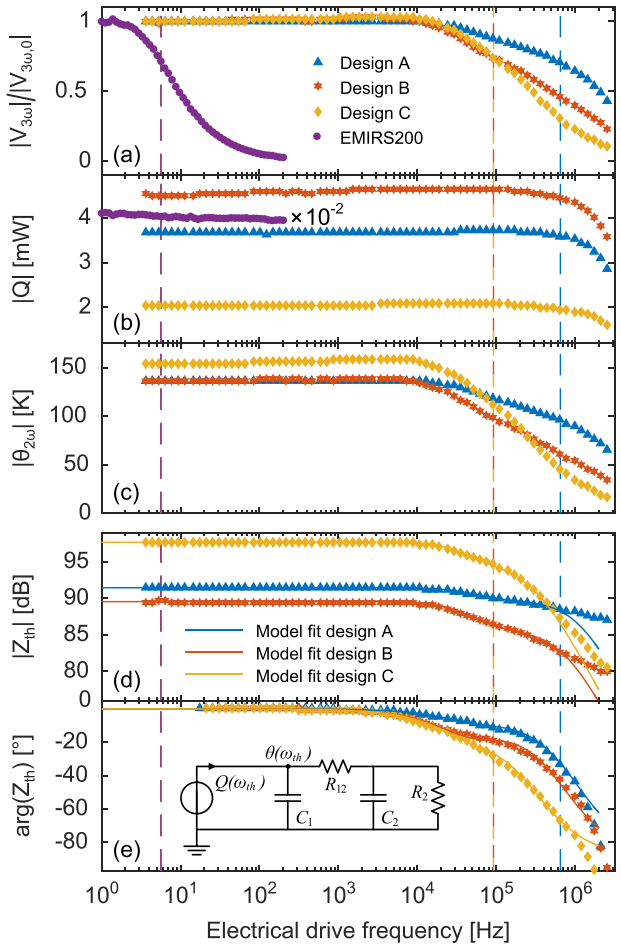

FIG. 3. The frequency response of: (a) the magnitude of the third harmonic component of the voltage across the nanoheaters, normalized, (b) the magnitude of the applied heating power, (c) the amplitude of the temperature oscillation, (d) the magnitude on dB scale (referred to 1 K/W), and (e) the phase of the thermal impedance of the nanoheaters, with a schematic of the thermal system's model. The vertical dashed lines indicate the thermal cut-off frequencies. Note that the thermal frequency is twice the electrical drive frequency.

This is consistent with reported TCR values for evaporated Pt thin films.[7,14,20]

The frequency characterization experiment was performed with the substrate at room temperature, driving the nanoheaters with the AC circuit in Fig. 1. The current in the circuit was determined by measuring the voltage across the series resistance R_{series}. We measured the voltages across the nanoheaters and the series resistance with a lock-in amplifier (Zurich Instruments HF2LI) capable of measuring three harmonic components. We applied a fixed voltage amplitude, individually chosen for each device so as to give a low-frequency thermal oscillation amplitude of ∼150 K, i.e., temperature modulation between T_0 (room temperature) and $T_0 + 300$ K. The driving amplitudes for designs A, B, and C were 2.42 V, 2.98 V, and 1.87 V, respectively. As a comparison, we also measured the frequency response of the commercial millimeter-sized MEMS-based IR source EMIRS200 (Axetris AG, Switzerland).

Finally, we evaluated the effect of the large temperature oscillation amplitude on the measured nanoheater properties. We performed the same measurement of current and voltage described above, now varying the applied voltage amplitude, at the fixed low frequency of 523 Hz, chosen to avoid the 50 Hz power line disturbance and its harmonics.

Fig. 3 displays the frequency responses of the nanoheaters and the EMIRS200. Panel (a) shows the normalized third harmonic component of the voltage across each device. The difference in frequency range between the EMIRS200 and the nanoheaters is vast. The EMIRS200 has a thermal cut-off frequency of 11 Hz, while the nanoheaters are four to five orders of magnitude faster. To correctly analyze their high-frequency behavior, one has to account for any frequency dependence of the applied heating Q. As shown in panel (b), the heating power gradually drops above 100 kHz because of parasitic reactances in the drive circuit. Panel (c) shows the nanoheaters' temperature oscillation, derived with Eq. (4). All the nanoheaters exhibit a low-frequency oscillation amplitude of about 150 K, as targeted, while their high frequency behavior differs. Finally, we apply Eq. (1) to obtain the complex thermal impedance of each design: its magnitude is plotted on a dB scale in panel (d) and its phase in panel (e).

We quantify the thermal bandwidth by the thermal cut-off frequency values $f_{\text{th},-3\text{dB}}$, listed in Table I, at which the magnitude of the thermal impedance drops to $1/\sqrt{2}$ of its low frequency value. However, because there are multiple layers with different thermal properties under the Pt nanoheater, we do not expect the devices to exhibit a simple first order response. We find that a second order RC ladder, schematized in panel (e), provides a good fit to our observations up to 1 MHz. The impedance function of this model is

$$Z_{\text{mod}}(\omega_{\text{th}}) = \frac{R_{12} + R_2 + j\omega_{\text{th}} R_{12} R_2 C_2}{1 - \omega_{\text{th}}^2 R_{12} R_2 C_1 C_2 + j\omega_{\text{th}}((R_{12} + R_2)C_1 + R_2 C_2)}. \quad (5)$$

Its magnitude and phase are plotted as solid lines in panels (d) and (e), respectively. Table I lists the fitted parameters C_1, R_{12}, C_2, and R_2 for each design. We interpret C_1 as the effective heat capacitance (thermal mass) of the Pt nanoheater plus a volume of thermally communicating material below it.

TABLE I. Measured parameters—Electrical resistance at room temperature R_0, thermal cut-off frequency $f_{\text{th},-3\text{dB}}$, thermal resistance R_{th}, and rate of variation of the normalized thermal conductance with temperature $\Delta G_{\text{th}}/\Delta T$ – and fitted parameters–C_1, R_{12}, C_2, and C_2–for the three nanoheater designs and the Axetris EMIRS200.

Design	R_0[Ω]	$f_{\text{th},-3\text{dB}}$ [MHz]	R_{th} [K/mW]	$f \cdot R$ [MHz K/mW]	$\Delta G_{\text{th}}/\Delta T$ [%/K]	C_1 [pJ/K]	R_{12} [K/mW]	C_2 [pJ/K]	R_2 [K/mW]
A	35	1.3	37	48	0.055	2.5	31	220	6.8
B	31	0.18	30	5.4	−0.15	6.1	19	180	11
C	34	0.18	77	14	−0.18	5.3	54	85	22
EMIRS200	39	1.1×10^{-5}	…	…	…	…	…	…	…

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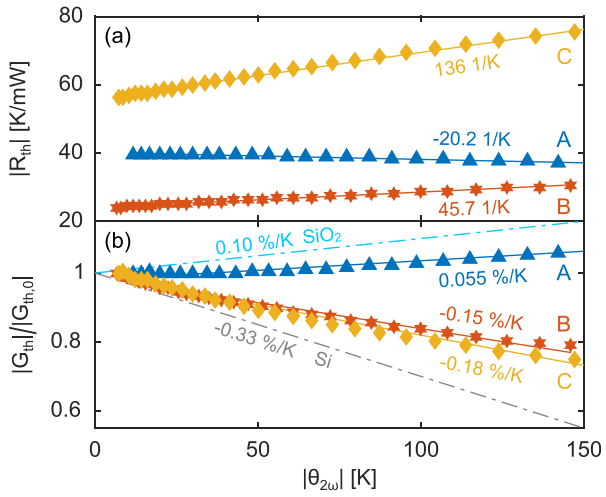

FIG. 4. (a) The total low frequency thermal resistance R_{th} and (b) the normalized thermal conductance, as functions of the amplitude of the temperature oscillation $\theta_{2\omega}$. The solid lines show linear fits and the dashed light blue and gray lines show the expected slopes for bulk SiO_2 and Si, respectively.

From geometry and material data,[17] we calculate a 0.3 pJ/K contribution of the Pt nanoheater itself to C_1. In design A, the upper thermally insulating SiO_2 layer confines the heat; therefore, only a small volume of underlying material contributes to C_1. This explains design A's smaller C_1, compared to designs B and C. R_{12} represents the thermal resistance between the fast-heating volume of material represented by C_1 and the thermally slower volume of material represented by C_2. R_2 finally describes the spreading of the heat to the thermally invariant volume of material. R_{12} and R_2 are highest in design C, where the spreading of the heat is hindered sideways by the removal of large parts of the Si layer and downwards by the air gap under the Si. The absence of the thick SiO_2 layer also explains design C's smaller C_2. In design B, R_{12} mainly describes the spreading of the heat from the fast-heating volume sideways in the Si layer. The similarity of design B's C_1 to that of design C indicates that the fast-heating volume is laterally confined close to the Pt nanoheater. This implies that most of the Si layer is thermally slower than the heater and thus contributes to C_2, together with the thick SiO_2 layer.

Fig. 3(d) also shows that, due to its thermal isolation, design C is more power-efficient than designs A and B. Compared to design A, this comes at the expense of bandwidth. Design A, in fact, has the highest bandwidth–thermal resistance product $f \cdot R$, as listed in Table I.

Fig. 4(a) displays the low-frequency thermal resistance R_{th}, corresponding to $R_{12} + R_2$ in the fitted model, as a function of the temperature oscillation amplitude. Fig. 4(b) shows the normalized thermal conductance G_{th}, obtained by inverting and normalizing R_{th}. The variation of these parameters with temperature is below 20%. Furthermore, we observe that R_{th} increases with temperature for designs B and C, while it decreases for design A, and that the trends of $|G_{th}|$ are the ones expected according to our above analysis, considering the rates of variation of the thermal conductances of pure SiO_2 and Si, also plotted in Fig. 4(b). This further supports our interpretation of R_{12} and R_2.

We presented three fast Pt nanoheater designs and characterized their thermal impedance up to MHz frequencies. Furthermore, we fitted a lumped-element thermal model to our data and identified the physical properties associated with the model's thermal capacitances and resistances. We showed that these properties can be engineered by nanostructuring the substrate supporting the Pt nanoheaters, and we demonstrated that our fastest design has a thermal cut-off frequency of 1.3 MHz, corresponding to a thermal time constant of 0.769 μs, and a thermal resistance of 37 K/mW, yielding a $f \cdot R$ product of 48 MHz K/mW. Our results show that the small thermal mass of these nanoheaters makes them ideal as power-efficient, electrically driven sources of heat and radiation that enable the resolution of dynamics up to MHz frequencies, e.g., in on-chip absorption spectroscopy and scanning probe thermography.

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