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Nanopore arrays in a silicon membrane for parallel single-molecule detection: fabrication

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Abstract

Solid state nanopores enable translocation and detection of single bio-molecules such as DNA in buffer solutions. Here, sub-10 nm nanopore arrays in silicon membranes were fabricated by using electron-beam lithography to define etch pits and by using a subsequent electrochemical etching step. This approach effectively decouples positioning of the pores and the control of their size, where the pore size essentially results from the anodizing current and time in the etching cell. Nanopores with diameters as small as 7 nm, fully penetrating 300 nm thick membranes, were obtained. The presented fabrication scheme to form large arrays of nanopores is attractive for parallel bio-molecule sensing and DNA sequencing using optical techniques. In particular the signal-to-noise ratio is improved compared to other alternatives such as nitride membranes suffering from a high-luminescence background.

Keywords: nanopore, parallel, single-molecule

(Some figures may appear in colour only in the online journal)

Introduction

One of the most basic requirements for life is a controlled cell metabolism, which is regulated by the biological cell membrane and its inherent protein pores with diameters in the range of a few nanometers. These nanopores act as passive gates to allow or inhibit the flow of ions, molecules, etc by chemical recognition or simply by spatial confinement. Making use of these selective characteristics, nanopores can be used as a sensor to extract information from translocating biological objects. Here, the subject of reading DNA is of particular interest as it might enable highly individualized medication by mapping the human genome. To be able to read the genome in reasonably short time, parallel DNA sequencing methods [1] are pursued, which allow a massive and high-throughput reading. Demanding for a homogenous, periodic distribution of sensors and pores that are small enough (~2 nm diameter range to ensure an accurate sensing of single DNA strands), an array of solid-state silicon-based nanopores seems to be a viable approach. Whereas the fabrication of Si devices containing an array of nanopores can be implemented in current existing microelectronics fabrication technology, the required small diameter, however, presents a tremendous challenge. Today's lithographical methods are restricted to sizes larger than ~10 nm, even using state-of-the-art electron-beam lithography. Therefore, nanopore fabrication was mainly focused on single pore drilling in the sub-10 nm range (on SiN or SiO_2 membranes) by using a focused electron beam [2–6] or a focused ion beam [7–9] and arrays were realized by drilling pores one by one, an inherently slow method. In order to fabricate larger arrays in an efficient way, attempts have been undertaken to prepare sub-10 nm pore arrays by shrinkage of larger openings (defined by lithography) by oxidation [10] or by atomic layer deposition [9]. Also other methods leading to randomly distributed nanopores have been tested [11].

Electrochemical etching is a promising technique to obtain deep, nanometer-wide pores at high aspect ratio. The etched area on a sample, at least in principle, scales with the etching current allowing the pore diameter to be reduced accordingly. It has been shown to be an advanced tool with which to fabricate a large variety of structures [12–16], in particular homogenous, high-aspect-ratio pore arrays in bulk silicon in the micrometer as well as in the sub-micrometer range [17–21]. Fabrication of pores in bulk-like silicon membranes using electrochemical etching was previously demonstrated in our group resulting in ~250 nm wide pores in ~30 μm thick membranes [22]. Létant *et al* [23] prepared relatively thick silicon membranes of 15 and 45 μm (etched into a rigid silicon wafer) with pore diameters ranging between 0.5 and 2 μm, respectively, and demonstrated selective capture of bio-organisms. Pores with diameters as small as 30 nm as a result of etching in the breakdown regime were achieved on μm-thick membranes [24]. However, the use of a silicon-on-insulator structure [25] (SOI wafer), enables very thin membranes to be formed which we believe is the key to form sub-10 nm pores by electrochemical etching.

In this paper we address the fabrication of large nanopore arrays on a silicon membrane, where membrane fabrication is based on the use of SOI wafers. Furthermore, in our two-step approach, positioning of the pores is entirely decoupled from the nanopore diameter: arrays are defined by conventional optical or electron-beam lithography. Pores are formed by a two-step etching process, consisting of anisotropic etching to form pyramidal etch pits which subsequently, at the apex, initiate nanopore formation using electrochemical etching. Pore size and depth are controlled electrochemically by the anodizing current and time in the HF etchant. Thus, we have been able to reach pores with diameters as small as 7 nm at 50–100 nm pore length fully penetrating the membrane. Such a simultaneous, multipore array fabrication method is advantageous compared to e-beam 'drilling' techniques and it enables parallel (optical) detection of (fluorophore-labeled) bio-molecules, as shown in a separate study in a companion paper [26].

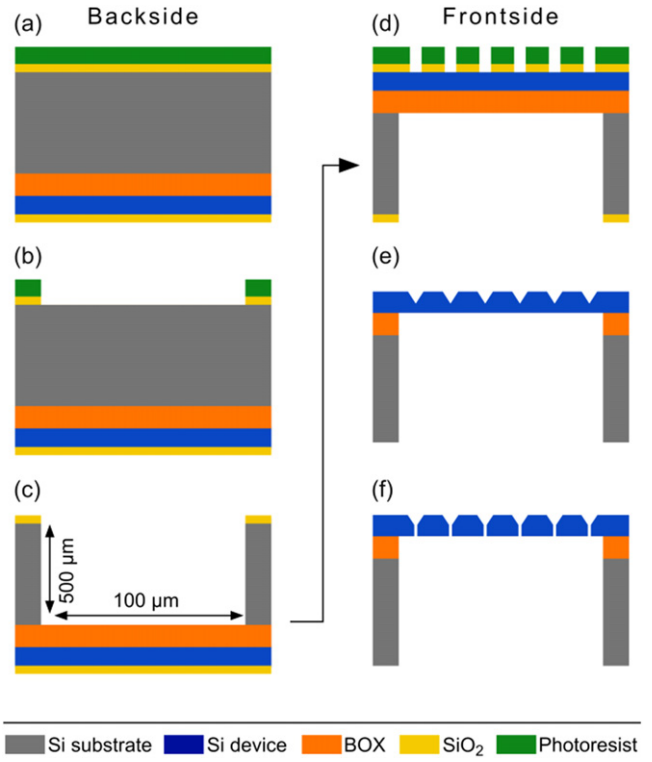

Figure 1. Schematic of membrane fabrication and frontside patterning. Wafer backside: (a) and (b) first the backside of the wafer is patterned by optical lithography to define an array of membranes which is then transferred to the oxide layer (here shown for one membrane). (c) By applying standard inductively coupled plasma etching, the oxide-embedded membranes are revealed. Wafer frontside: (d) an array of 10×10 squares is drawn on each membrane by e-beam lithography. (e) KOH etching and oxide removal in 5% HF are applied to obtain free-standing, patterned, bare silicon membranes. (f) Finally, electrochemical etching is performed on each membrane individually to form the nanopores.

Experimental details

Essential for membrane manufacture is the buried oxide (BOX) layer, which separates the device layer (which will form the Si membrane after processing) from the silicon substrate of the SOI wafer and acts as an etch stop for the backside-through-wafer etching. The related processing with standard cleanroom techniques is schematically depicted in figure 1. The initial SOI wafer (p-type (100), SOITEC) consists of a 340 ± 12.5 nm Si device layer (blue), a 400 nm BOX layer (orange) and a 520 μm Si substrate layer (grey). A 100 nm silicon oxide layer (yellow) on each side after an initial oxidation (consuming ~40 nm silicon) serves as a hard mask for etching. Starting on the wafer backside, an array of 32 membranes is defined on a 10 μm thick photoresist (AZ9260, AZ Electronic Materials) by optical lithography and is subsequently transferred to the silicon oxide layer. Using the Bosch process, backside trenches, each of them 520 μm deep and 100 by 100 μm^2 large, are then formed by inductively coupled plasma (ICP) etching (figures 1(b) and (c)). A cross-sectional micrograph of such a trench is shown in figure 2. Next, the membrane´s front side is structured in order to provide predetermined locations for nanopore growth by electrochemical etching. To do so, an array of squares (300×300 nm^2) is written on positive resist Zep520 using e-beam lithography and is then transferred by reactive ion etching to the top oxide layer of the oxide-embedded membrane (figure 1(d)). Following alkaline wet etching in 30% KOH at 80 °C for 90 s and subsequent removal of the oxide in 5% HF, a free-standing silicon membrane with an array of inverted pyramids is obtained (figure 1(e)). In a last step (f), nanopores are subsequently formed by anodic etching of the remaining Si in hydrofluoric (HF) acid. The thickness of the remaining silicon, which is given by the distance between the inverted pyramid tip (the bottom of the etching pit) and the backside of the membrane, defines the length of the electrochemically etched pore. Taking into account that the depth of the pyramid is $1/\sqrt{2}$ of the width, the pore length is estimated to be in the range between 50–100 nm, depending on the local thickness variation of the SOI device layer and the variation of the pyramid size induced by lithography. Since this last etching

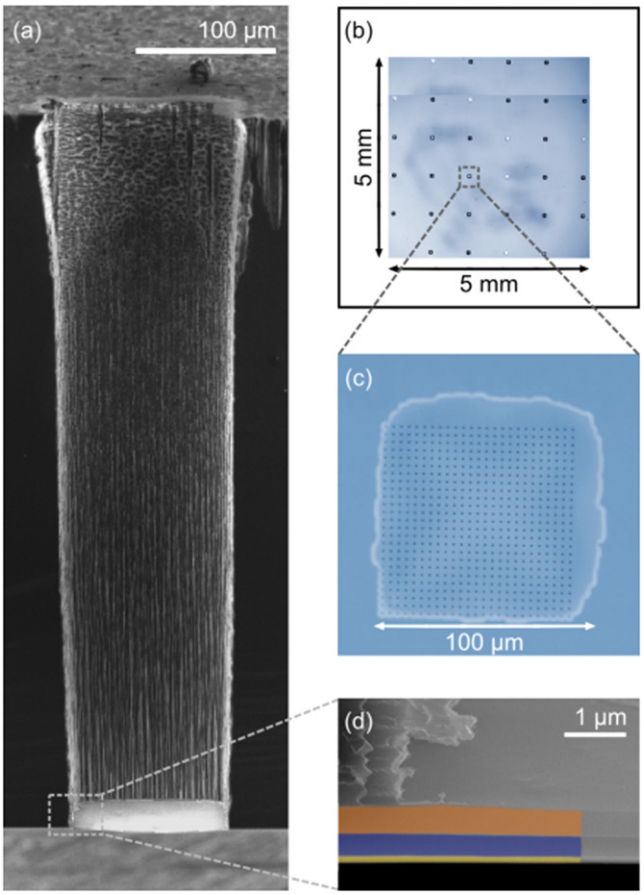

Figure 2. (a) Cross-sectional scanning electron microscope (SEM) micrograph of a trench with a membrane located at the bottom of the trench. The according zoom-in of the area indicated by the dashed rectangle in (a) is shown in (d). Here, the Si membrane (blue) is still embedded in silicon dioxide (yellow/orange). The SEM image is partly colorized according to the scheme shown in figure 1. (b) Photograph of a silicon chip containing 32 membranes with 1 mm spacing. (c) Optical microscope image of a typical $100 \times 100\,\mu m^2$ large membrane with an array of inverted pyramids on the front side.

step is vital for the realization of well-defined pore arrays, we will take a closer look at the experimental conditions as well as at the process of nanopore formation in the following.

A schematic of the home-built etching cell (partly based on the design of Etch and Technology GmbH, Germany) implemented for electrochemical etching on Si membranes is shown in figure 3. Due to the fact that the membranes are suspended within an insulating SOI structure, a double cell is necessary in order to realize electrical contact directly on the membranes backside (by the electrolyte). The etching cell setup is completely built-up out of solid polytetrafluoroethylene (PTFE). Voltage is applied using a potentiostat (model VersaSTAT 4, Princeton Applied Research) equipped with a low-current interface (LCI, VersaSTAT LC) providing a minimum current range of several pA with aA (10^{-18}) current resolution. As indicated in figure 3, the aqueous etchant flows continuously across the wafer frontside, providing steady removal of hydrogen bubbles, constant HF concentration, and a homogeneously etched surface. For circulation a peristaltic pump from Ismatec (pump drive: model

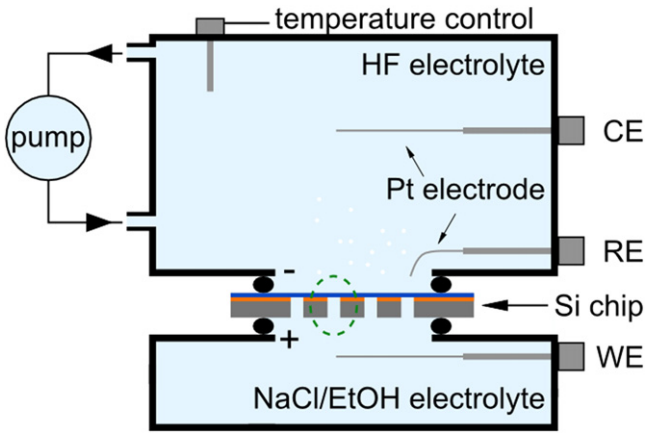

Figure 3. Schematic of the etching double cell. The Si chip containing 32 membranes (not to scale) is mounted between the lower and upper part of the etching cell. As an example, one membrane is encircled by a green dashed line. CE: counter electrode, WE: working electrode, RE: reference electrode.

MCP-process ISM915A IP65, pump-head: model ISM734B) is used. In addition, the temperature of the electrolyte is kept constant by a standard thermostat-controlled circulating water bath.

The silicon chip of $1.5 \times 1.5\,cm^2$ size, which carries 32 membranes, is placed between the upper and lower compartment of the etching cell. Via the electrolytes the electric circuit is then closed by the potentiostat. Etching is carried out by applying a constant bias in standard three-electrode configuration, which allows monitoring of the etching current without load. In this way, controlled etching of nanometer-wide pores is possible, as was recently demonstrated on bulk silicon [17]. For the etchant, a mixture of 50% hydrofluoric acid, ethanol and deionized water (1:3 ratio) is used and balanced to a concentration of 5.4 wt% HF and kept at a constant temperature of 5 °C. Note that in order to inhibit etching on the membrane backside, a HF-free NaCl ethanol mixture is used as electrolyte in the lower cell compartment.

Results and discussion

Figure 4 shows a typical scanning electron microscope image (SEM: Gemini, ULTRA 55, Zeiss) of a membrane after electrochemical etching was carried out. The 10×10 array depicted here contains sub-20 nanometer-wide pores, which are located in the center of the pyramidal pits. SEM images were recorded of each individual pyramidal pit and were analyzed (with Digital Micrograph software). Pores were observed at about 20% of the pyramids. The resulting size distribution is plotted in the lower panel of figure 4 and reveals a narrow distribution of pore diameters peaking at ~10 nm (FWHM ~6 nm). The smallest pore observed here is ~7 nm in diameter.

The underlying mechanism of nanopore formation is illustrated in figure 5. Here the particular case of a Si membrane is sketched for one pyramidal pit in the cross section and in the top view at different stages of etching (time

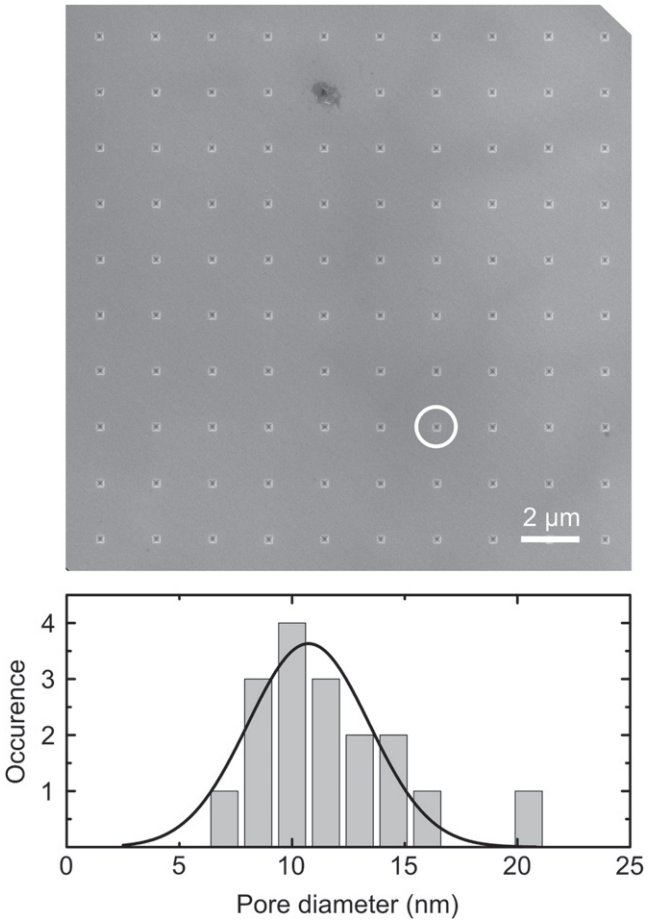

Figure 4. Scanning electron micrograph of a Si membrane showing a 10 by 10 array with 2 μm pitch distance after electrochemical etching (anodization time 75 s). Nanopores were observed at about 20% of the pyramidal trenches. The according size distribution is plotted below. Assuming a Gaussian distribution, the average pore diameter is 11 nm. The smallest diameter observed on this array is as small as 7 nm.

intervals). The scheme in the lower panel is based on the electrochemical dissolution reaction taking place in bulk silicon [27] and modified according to our observations made on different membranes with different pore sizes. A representative set of our observations (SEM micrographs), selected for discussion, is shown in the upper panel. From left to right, higher magnification scans of individual pyramidal pits are depicted, where figure 5(a) is before etching while following images are after increasingly longer (figure 5(b) 75 s, (c) 200 s, and (d) 600 s) etching times resulting in pore diameters of 11 nm, 30 nm, and 200 nm, respectively. Note that the image in figure 5(b) was taken from the inverted pyramid marked with a white circle in figure 4. As can be observed, longer anodization times in HF lead to a successive enlargement of the pore diameter and the geometrical pyramidal structure gradually vanishes. This observation can be explained as follows. First, when brought in contact with HF electrolyte, before applying any bias, charge transfer at the interface is observed due to alignment of the semiconductor Fermi energy level with the chemical potential of the liquid till equilibrium. As a consequence, a space charge region (SCR) is formed within the silicon, which is depleted of mobile charge carriers. In the case of moderately doped p-type silicon, i.e. a resistivity of 20 Ω cm, as it is used for membrane fabrication, the SCR extends over several micrometers leading to full depletion of the 300 nm thick membrane. Thus, the common way of performing electrochemical etching (under forward conditions, i.e. anodically biased) by supplying holes from the non-depleted bulk region adjacent to the SCR will not work. In order to initiate etching, an external potential, high enough to generate electron–hole pairs by electrical breakdown [20], is applied across the membrane. Taking into account the breakdown field strength in silicon ($\sim 3*10^5$ V cm^{-1}), a voltage of 10–15 V is sufficient to reach breakdown conditions on 300 nm thick silicon, in particular at the pyramidal apex where the effective membrane thickness is much reduced. Note that applying the right bias is a sensitive task, since too-high voltages simply cause total loss of the membranes by rupture. The positive charge carriers are then attracted and forced towards the Si/HF-electrolyte interface. Si–Si bonds, which are weakened by the nucleophilic attack of fluoride ions, break and surface atoms are removed. To achieve a controlled, local dissolution, i.e. pore formation at distinct distances, pre-patterning of the surface with an array of inverted pyramids is critical. Thus electrical breakdown (tunneling) occurs preferentially at the tips and pore growth is initiated at the pyramid's tip. Applying short etching times of several 10 s (see figures 5(b) and (c)) enables fabrication of nanometer-wide openings. But, as observed on the membrane shown in figure 4, only a fraction of the pyramids result in a nanopore, most probably due to a non-homogenous field distribution across the membrane caused by local variations (dopant distribution, proximity effects in lithography, bulging of membrane). When the etching is continued for several minutes, larger pores like the one in figure 5(d) are observed on each pyramidal pit. However, exceeded etching (long anodization times) results in merging of neighboring pores and thus loss of array character. Finally, to increase the fraction of successfully etched pores we tried to use a pulsed voltage but no clear difference could be observed compared to a constant voltage.

In order to prove that the as-etched pores penetrate throughout the entire thickness of the membrane, the backside of the membranes was investigated. Imaging of the backside was realized by an exfoliation method where the membrane is released from the chip simply using sticky tape. For reasons of visibility, a membrane with larger pores (each about 50 nm in diameter; see inset of figure 6) was chosen. Observing the micrograph in figure 6 carefully, a pattern of circular, equidistant spots (black spots, each highlighted by a white circle and array highlighted by dashed lines) can be recognized. This is indeed the characteristic of the array defined on the frontside with 2 μm pitch distance. Further efforts were undertaken to obtain images from membranes with smaller pores by transmission electron microscopy (TEM: JEM 2100F (HR), JEOL Electron Microscope 2100 Field, JEOL). For this purpose, parts of a membrane were extracted by focused ion beam technique (FIB: QUANTA 3D FEG, FEI) and then transferred to TEM copper grids. The results from

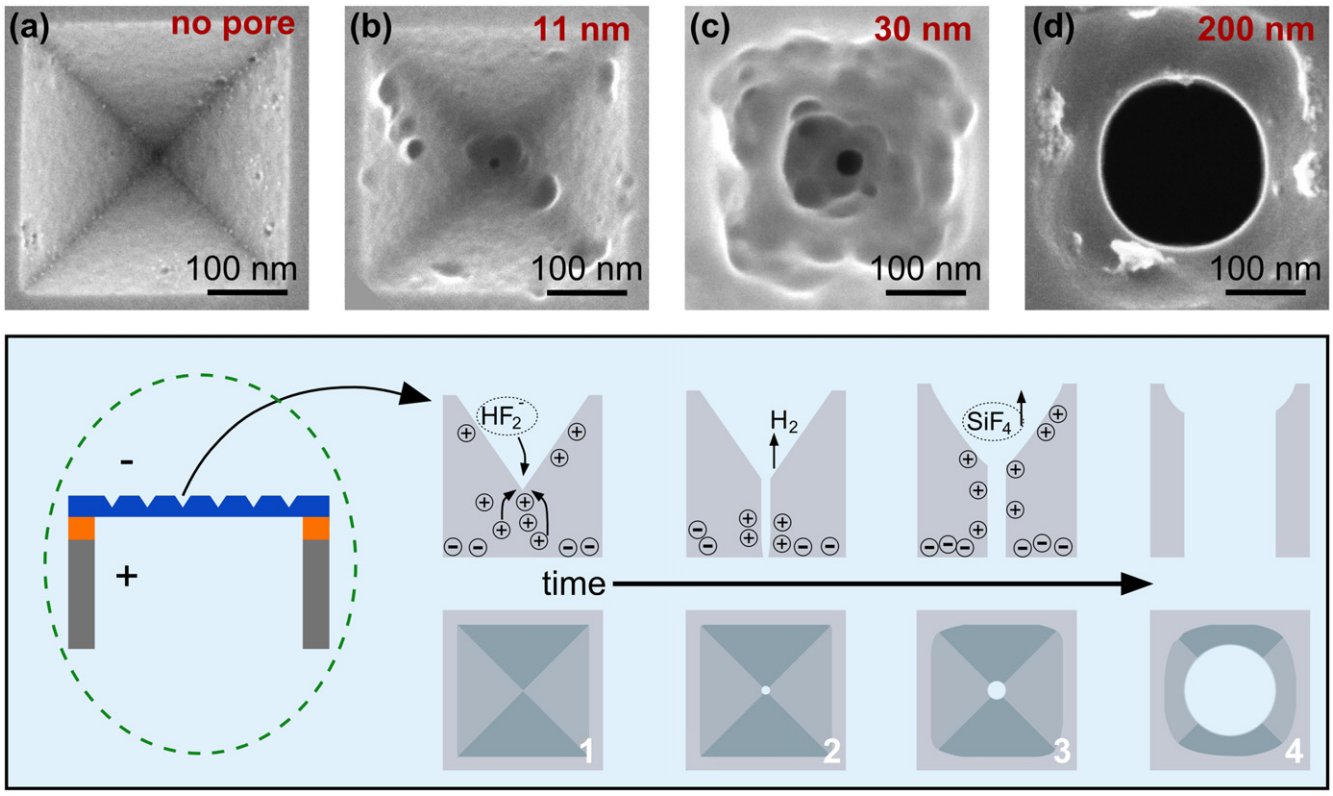

Figure 5. Upper panel: SEM micrographs of individual pyramids (a) before and (b)–(d) after electrochemical etching at progressively longer times; the longer the etching time, the larger the diameter. Lower panel: scheme of pore formation in a p-type Si membrane during anodic etching in HF.

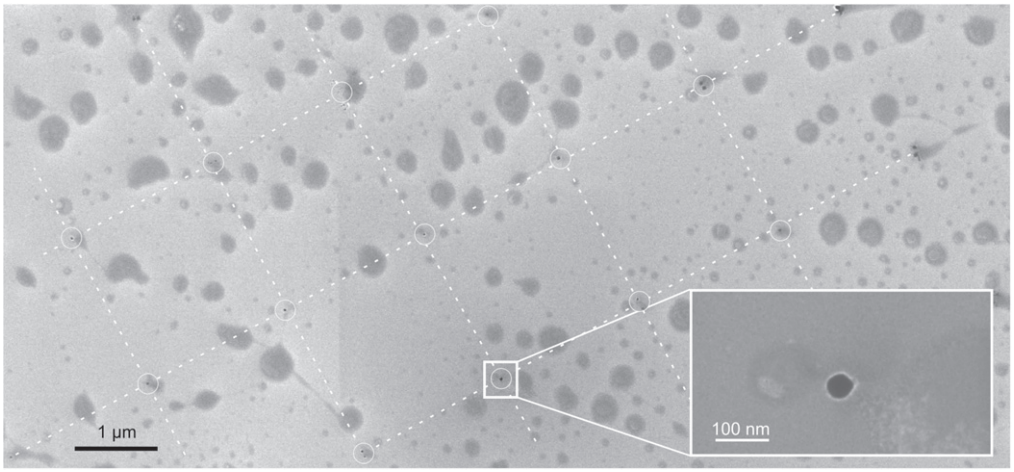

Figure 6. SEM micrograph of a membrane backside proving that the as-etched pores fully penetrate the entire membrane. Double pores were observed occasionally, probably due to formation of spiking pores (breakdown etching) and irregularity of the pyramids induced by lithography. The larger randomly positioned etch pits most likely stem from incomplete processing.

TEM imaging (not shown) confirm the stated nanopore size values.

The membranes were patterned with arrays of different pitch distances in order to evaluate its impact on the etching result. Membranes with 1 μm, 2 μm, 4 μm and 8 μm pore-to-pore distances were studied. No relevant influence on pore formation by electrochemical etching was observed. Well-separated nanopores are of particular interest for optical read-out approaches [28, 29], which allow parallel simultaneous detection of DNA translocation events and thus high analyte throughput. The performance of our nanopore membranes was investigated by translocation measurements of single fluorophore-labeled DNA strands in a wide-field microscope and is subject of a separate companion paper [26]. However, it turned out that for accurate optical read-out the high aspect ratio of the pores is beneficial and that larger pore-to-pore distances are preferred (e.g. 8 μm pitch distance).

Conclusions

In summary, we have demonstrated the fabrication of sub-10 nm nanopore arrays on silicon membranes by electrochemical etching. In this approach positioning of the pores, managed conveniently by lithographical techniques, is entirely decoupled from the nanopore diameter due to a separate etching step. Pore size and depth can be controlled electrochemically by the anodizing current and time in the HF etchant. Thus, nanopores with diameters as small as 7 nm were obtained. The pores (with a length of 50–100 nm) fully penetrate the membrane thickness as observed by imaging the backside of the membrane. The as-prepared nanopore arrays with distinct pore-to-pore distances are attractive for high throughput parallel biomolecule sensing and DNA sequencing using optical techniques. The low background luminescence of silicon membranes is here an important advantage compared to nitride membranes [30], enabling single fluorophore detection. In future, etching will be extended to n-type Si membranes in order to address the presently quite large variation in pore diameter. Here, better control of the electrochemical etching process is possible due to backside illumination [17], which may reduce both the pore size and its variation. Concerning the aspect of mass-fabrication of such nanopore arrays, the fabrication process can be scaled up by the use of optical instead of e-beam lithography on device layers of appropriate thickness (for SOI wafers).

Acknowledgments

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